WHAT IS CLAIMED IS:

1. A liquid crystal display panel comprising:

a plurality of gate lines and gate electrodes formed on a first substrate;

a gate insulating film formed on the first substrate including the gate lines and the gate electrodes;

a semiconductor film formed in a region on the gate insulating film;

an ohmic contact film formed on the semiconductor film;

a plurality of data lines formed in a crossing pattern with the gate lines;

a source electrode formed on the ohmic contact film;

a pixel electrode formed in a pixel region defined by the gate and data lines; and

a drain electrode formed on the ohmic contact film, and having an uneven width.

2. The liquid crystal display panel of claim 1, wherein the drain electrode has a first portion and a second portion, the first portion having a smaller width than the second portion of the drain electrode.

3. The liquid crystal display panel of claim 2, wherein the second portion directly contacts the pixel electrode.

4. The liquid crystal display panel of claim 2, wherein the first portion has a width substantially the same as the source electrode.

5. The liquid crystal display panel of claim 1, wherein the drain electrode has first, second and third portions, the second portion connecting the first and third portions, and the second portion being narrower in width than the first and third portions.

6. The liquid crystal display panel of claim 5, wherein the third portion directly contacts the pixel electrode.

7. The liquid crystal display panel of claim 5, wherein the first portion has a width substantially the same as the source electrode.

8. The liquid crystal display panel of claim 1, wherein the drain electrode has first and second portions, the first portion and second portions overlapping with the gate electrode and the second portion connected to the pixel electrode, the second portion having a smaller width than the first portion.

9. The liquid crystal display panel of claim 1, wherein the drain electrode has first, second and third portions, the first portion and second portions overlapping with the gate electrode and the third portion connected to the pixel electrode, the second portion having a smaller width than the first and third portions.

10. The liquid crystal display panel of claim 1, further comprising a passivation film formed on the entire surface of the first substrate.

11. The liquid crystal display panel of claim 1, further comprising an alignment film formed on the entire surface of the first substrate.

12. The liquid crystal display panel of claim 11, wherein the alignment film is formed by one of a rubbing method and a photo-alignment method.

13. The liquid crystal display panel of claim 1, wherein a region of the passivation film is exposed to form a contact hole.

14. The liquid crystal display panel of claim 13, wherein the pixel electrode is connected with the drain electrode through the contact hole.

15. The liquid crystal display panel of claim 1, further comprising a second substrate opposing the first substrate, wherein a black matrix and a color filter are formed on the second substrate.

16. The liquid crystal display panel of claim 15, wherein a liquid crystal layer is formed between the first and second substrates.

17. The liquid crystal display panel of claim 1, wherein the gate insulating film includes one of silicon nitride and silicon oxide.

18. The liquid crystal display panel of claim 1, wherein the data line, the source electrode, and the drain electrode include one of Al, Mo, Cr, Ta, and Al alloy.

19. A liquid crystal display panel comprising:

a plurality of gate lines and gate electrodes on a substrate;

a semiconductor film on the plurality of gate lines and gate electrodes;

a plurality of data lines in a crossing pattern with the gate lines;

a pixel electrode in a pixel region defined by the gate and data lines;

a drain electrode on the ohmic contact film, having an uneven width and having first and second portions,

wherein a second portion of the drain electrode has a smaller width than the first portion of the drain electrode; and

wherein the first and second portions of the drain electrode overlap with the gate electrode and the second portion is connected with the pixel electrode.

20. A liquid crystal display panel comprising:

a plurality of gate lines and gate electrodes on a substrate;

a semiconductor film on the plurality of gate lines and gate electrodes;

a plurality of data lines in a crossing pattern with the gate lines;

a pixel electrode in a pixel region defined by the gate and data lines;

a drain electrode on the ohmic contact film, having an uneven width and having first, second and third portions,

wherein the second portion of the drain electrode has a smaller width than the first and third portions of the drain electrode; and

wherein the first and second portions of the drain electrode overlap with the gate electrode and the third portion is connected with the pixel electrode.

21. A thin film transistor comprising:

a gate line and data line arranged on a substrate in first and second directions to define a pixel region;

a thin film transistor in a crossing point between the gate line and the data line; and

a drain electrode connected to a pixel electrode in the pixel region;

wherein the drain electrode has an uneven width.

22. A thin film transistor comprising:

a substrate;

a gate electrode on the substrate;

a gate insulating film on the gate electrode;

a semiconductor film and ohmic contact film on the gate insulating film;

a source electrode and a drain electrode on the ohmic contact film; and

a pixel electrode connected to the drain electrode;

wherein a first and second portions of the drain electrode overlap with the gate electrode and a second portion is connected with the pixel electrode, the second portion having a smaller width than the first portion.

23. A thin film transistor comprising:

a substrate;

a gate electrode on the substrate;

a gate insulating film on the gate electrode;

a semiconductor film and ohmic contact film on the gate insulating film;

a source electrode and a drain electrode on the ohmic contact film; and

a pixel electrode connected to the drain electrode;

wherein a first and second portion of the drain electrode overlap with the gate electrode and a third portion is connected with the pixel electrode, a second portion having a smaller width than the first and third portions.

24. A method of making a liquid crystal display panel comprising the steps of:

forming a plurality of gate lines and gate electrodes on a substrate;

forming a gate insulating film on the substrate including the gate lines and the gate electrodes;

forming a semiconductor film in a region on the gate insulating film;

forming an ohmic contact film on the semiconductor film;

forming a plurality of data lines in a crossing pattern with the gate lines;

forming a source electrode on the ohmic contact film;

forming a pixel electrode in a pixel region;

defining by the gate and data lines; and

forming a drain electrode on the ohmic contact film;

wherein the drain electrode has an uneven width.

25. The method of claim 24, wherein a first portion of the drain electrode has a smaller width than a second portion of the drain electrode.

26. The method of claim 24, wherein a second portion of the drain electrode has a smaller width than a first portion and a third portion.

27. The method of claim 24, wherein a first and second portion of the drain electrode overlap with the gate electrode, and the second portion is connected with the pixel electrode, the second portion having a smaller width than the first portion.

28. The method of claim 24, wherein a first and second portion of the drain electrode overlap with the gate electrode, and a third portion is connected with the pixel electrode, the second portion having a smaller width than the first and third portions.

29. The method of claim 24, wherein the gate lines and gate electrodes are formed by a sputtering method and then patterned using a mask.

30. The method of claim 24, wherein the gate insulating film is formed by a chemical vapor deposition (CVD) process.

31. The method of claim 30, wherein the gate insulating film includes one of silicon nitride and silicon oxide.

32. The method of claim 24, wherein the data line, the source electrode and the drain electrode include one of Al, Mo, Cr, Ta, and Al alloy.